

WHAT IS CLAIMED IS:

1. A method of fabricating an integrated circuit, the method comprising:

forming a barrier layer along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects a first conductive layer and a second conductive layer;

forming a seed layer proximate and conformal to the barrier layer; and

ion implanting elements into the seed layer.

2. The method of claim 1, wherein ion implanting elements into the seed layer comprises low energy ion implanting elements into the seed layer.

3. The method of claim 1, further comprising selectively controlling concentration of the implanted elements.

4. The method of claim 1, wherein the ion implanting is at an energy level of 0.25 to 20.0 KeV.

5. The method of claim 1, wherein the ion implanting is at a concentration of $1\text{E}15$ to $1\text{E}17$ atoms/cm².

6. The method of claim 1, further comprising tilting the integrated circuit thereby controlling placement of the implanted element on lateral side walls and the bottom of the via aperture.

7. The method of claim 1, wherein the implanted element includes a copper (Cu) alloy.

8. The method of claim 1, wherein the seed layer has a cross-sectional thickness of between 50 and 1,000 Angstroms.

9. The method of claim 1, wherein the seed layer is formed by an angle implant to achieve a uniform distribution of elements.

5 10. A method of implantation after copper seed deposition in an integrated circuit fabrication process, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing a conformal layer at a bottom and sides of a via
10 aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

providing an ultra-low energy ion implant to form a seed layer over the conformal layer;

filling the via aperture with a via material; and
15 providing a second conductive layer over the via material such that the via material electrically connects the first conductive layer to the second conductive layer.

11. The method of claim 10, wherein providing an ultra-low energy ion implant to form a seed layer over the conformal layer includes
20 implanting a plurality of elements into the seed layer.

12. The method of claim 10, wherein providing an ultra-low energy ion implant to form a seed layer over the conformal layer includes providing an implant concentration of $1\text{E}15$ to $1\text{E}17$ atoms/cm².

13. The method of claim 10, wherein providing an ultra-low
25 energy ion implant to form a seed layer over the conformal layer includes providing an implant depth of 50 to 1,000 Angstroms.

14. The method of claim 10, wherein the seed layer has a cross-sectional thickness of 50 to 1,000 Angstroms.

15. A method of forming a via in an integrated circuit, the method comprising:

- 5 depositing a first conductive layer;
- depositing an etch stop layer over the first conductive layer;
- depositing an insulating layer over the etch stop layer;
- forming an aperture in the insulating layer and the etch stop layer;
- 10 providing a barrier material at a bottom and sides of the aperture to form a barrier layer;
- providing a seed layer over the barrier layer;
- providing a controlled low energy ion implantation into the seed layer;
- 15 filling the aperture with a via material.

16. The method of claim 15, wherein the ion implantation is at an angle of between 35 and 90°.

17. The method of claim 15, wherein control of ion implantation includes tilting the seed layer.

20 18. The method of claim 15, wherein the ion implantation into the seed layer includes B, P, or Ge elements.

19. The method of claim 15, wherein the barrier layer is Ta, TaN, or TiN.

20. The method of claim 15, wherein the ion implantation is
25 controlled by the implantation energy ranging from 0.25 to 20.0 KeV.